

Xerox Docket No. D/A1591D

**PATENT APPLICATION**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Jingkuang CHEN et al.

Group Art Unit: 2813

Application No.: 10/727,692

Examiner: Nema A. Berezny

Filed: December 4, 2003

Docket No.: 111517.01

For: SYSTEMS AND METHODS FOR INTEGRATION OF HETEROGENEOUS  
CIRCUIT DEVICES

**DECLARATION UNDER 37 C.F.R. §1.131**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

We, Jingkuang Chen and Yi Su, hereby declare and state that:

1. This Declaration is submitted as evidence that the invention of this application was invented by us prior to March 14, 2001, which is the effective filing date of U.S. Patent No. 6,546,798 to Waters et al., entitled "Micro-Electro-Mechanical Systems Resonant Optical Gyroscope," which was applied in the April 11, 2005 Office Action.
2. We are the named inventors in the above-identified application.
3. We are the inventors of the invention described in an invention proposal entitled "An IC Process For Integration Of CMOS With Lateral DMOS Photodiodes For Visible Lights," which appears as Exhibit A attached to this Declaration. The invention proposal is signed by us and dated February 23, 2001.
4. The copies of these pages which constitute Exhibit A are true copies of the invention proposal.

5. The invention described by Exhibit A was conceived and actually reduced to practice by us in the United States at least as early as February 23, 2001.

6. We were in possession of the invention recited in claims 1, 3-14 and 17-21 as evidenced by the entire disclosure of Exhibit A.

7. We hereby declare and state that all statements made herein of our own knowledge are true, and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine and/or imprisonment under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing therefrom.

Date: June 27, 2005

Jingkuang Chen  
Jingkuang Chen

Date: \_\_\_\_\_

\_\_\_\_\_  
Yi Su

Attachment:  
Exhibit A



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Date: \_\_\_\_\_

Date: 6/24/05

\_\_\_\_\_  
Jingkuang Chen

Yi Su  
Yi Su

Attachment:  
Exhibit A



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## Invention Proposal

RECEIVED

FEB 27 2001

THE DOCUMENT COMPANY

XEROX

IPA10283

KEVIN R. KEPNER

Signed hard copy To: Xerox Intellectual Property Law Department

☒ Xerox Square -20A, Rochester, NY 14644, MailStop XRX2-20A - Send electronic version to your mgr. & copy to: USA.IPLD.MC@mc.usa.xerox.com☐ El Segundo, CA, 1990 Xerox Centre Dr. 90245, MailStop ESC1-275 - Send electronic version to your mgr. & copy to: USA.IPLD.ES@mc.usa.xerox.com☐ Palo Alto, CA, 3333 Coyote Hill Road 94304, MailStop: PARC - Send electronic version to your mgr. & copy to: USA.IPLD.PA@mc.usa.xerox.com☐ Wilsonville, OR, 26600 SW Parkway 97070, MailStop: 7063-LAW Send electronic version to your mgr. & copy to: USA.IPLD.OR@mc.usa.xerox.com

1	Proposal Submitted By (Please use legal name) Full First Name, Middle, Last <b>Jingkuang Chen</b> <i>MSML</i>		Employee No. 983673	Outside Phone No. (716) - 422-2136
	Organization (Unit/Div./Dept./Section) <b>WCRT/MS&amp;ML/MEMS</b>	Electronic Mail Address <b>jchen@crt.xerox.com</b>	Bldg. No./ Mail Stop <b>147-16C</b>	Fax No.
2	Proposal Submitted By (Please use legal name) Full First Name, Middle, Last <b>Yi Su</b>		Employee No. X-06253	Outside Phone No. (716) 422-5018
	Organization (Unit/Div./Dept./Section) <b>WCRT/MS&amp;ML/MEMS</b>	Electronic Mail Address <b>Syi@crt.xerox.com</b>	Bldg. No./ Mail Stop <i>114-418</i>	Fax No.
3	Proposal Submitted By (Please use legal name) Full First Name, Middle, Last		Employee No.	Outside Phone No. ( ) - - -
	Organization (Unit/Div./Dept./Section)	Electronic Mail Address	Bldg. No./ Mail Stop	Fax No.

\* If space for additional submitters is required, please use another sheet; and attach any supplementary Comments.

Manager <b>Joel Kubby</b>	Electronic Mail Address <i>j.kubby@crt.xerox.com</i>	Bldg. No./MS <i>147-16A</i>
Technical Category (see attached list) <i>3.17, mems devices</i>	Name of Xerox Program (if any) <i>ATP/Optical MEMS</i>	

Opportunity for licensing revenue Who could be interested in it? How is this better than alternatives? *Higher level of integration*  
*Optoelectronics companies, optical MEMS companies, MEMS companies*

Descriptive title of invention

**An IC Process for Integration of CMOS with Lateral DMOS and photodiodes for Visible Lights**

Describe the problem How was this problem tackled before your invention?

Integration of low-voltage CMOS circuits with high voltage DMOS drivers and photodiodes is of critical importance in implementing MOEM systems for telecommunication and many other applications. Before because of lack of such a technology, different IC chips (photodiodes, CMOS signal processing circuits, high voltage drivers) have to be wired bonded into an optical system to achieve the function of optical-electrical signal conversion/processing and control MEMS actuators. Such approached normally suffers from bulky size, inaccuracy, and high cost.

Summary of the invention Describe briefly what the invention is and how it works in 5-8 lines.

This invention describes an IC process that monolithically integrates low voltage CMOS circuits with high voltage DMOS drivers and photodiodes for visible wavelength.

The following process flow will be disclosed to our ATP partner standard MEMS. They have certain licensing rights to the process as described in the ATP Collaborative Agreement

Witnessed and Understood By <i>Joel Kubby</i>	Date <i>2/23/01</i>
Submitter(s) Signature(s) <i>Jingkuang Chen Yi Su</i>	Date <i>2/23/01</i>



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**Describe your invention** Describe how to make and use the invention and its novel embodiments. Cover the process, method, materials with sketches, flow charts, usage etc. What are the advantages of your invention for Xerox?

**CMOS/DMOX/Photodiode Integration**

Step	Description	Specifications	Target
1 Substrate	Scribe wafers for splits on a)HV n well implant, a1 and a2 b)p-body implant, b1, b2,b3 c)p-body annealing c1, c2, c3	4", <100>, p-Si, Boron doped, $1.0 \times 10^{15}/\text{cm}^3$ (10-20 ohm-cm) (start with 18 device wafers)	
2 Prefurnace clean	(add 3 monitoring wafers)	Standard RCA clean	
3 masking oxide growth for well Implantation	*add one monitor wafers	C2, DWD/TCA (DWDSKIN) Grow skin oxide: 800 degree C, 1 hr, dry O2 1100 degree C, 5-5-70-5-5 (set-dry1-wet/tea-dry2-N2anneal) TCA: LoN2=30sccm Standard ramp: Ramp up:10 degree C/min Ramp down:max Upgas:N2-3 Downgas:N2-3	7000 angstrom
	Inspect thickness (Ellipsometer)		
4 mask #1, HV n-well		a) bake 110 degree C, 15 min. b)HMDS, 4.0K, 30 sec. c)AZ 1813, 4.0K, 30 sec, 1.3um d)softbake, 90 degree C, 30 min e)expose, 5.0mW/cm2, 12 sec f) develop MF319, 1 min g)rinse DI water 5 min, spin dry h)hardbake 110 degree C, 15 min.	
5 Etch Oxide		BHF, 7-8 min DI water rinse, 5 minutes spin dry	1060 angstrom/min

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Submitter(s) Signature(s)	Date



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**6 Ion Implant High voltage n-well**

(leave PR on during implantation)

(add two monitoring wafers in the ion implantation)

two splits:

2.5e12/sq, Phos, 90keV

**7 Strip photoresist**

a) Hot PRS 2000, 30 minutes

(check under microscope)

b) rinse in DI water for 5 min, spin dry

**8 Mask #2, LV n-well**

a) bake 110 degree C, 15 min.

b) HMDS, 4.0K, 30 sec.

c) AZ 1813, 4.0K, 30 sec, 1.3um

d) softbake, 90 degree C, 30 min

e) expose, 5.0mW/cm<sup>2</sup>, 12 sec

f) develop MF319, 1 min

g) rinse DI water 5 min, spin dry

h) hardbake 110 degree C, 30 min.

**9 Etch Oxide**

BHF, 7-8 min

DI water rinse, 5 minutes

1060  
angstrom/min

**10 Ion Implantation Low voltage n-well**  
(add one blank monitoring wafer)

8.0e12/sq on ALL wafers

**11 Strip photoresist**

a) Hot PRS 2000, 30 minutes

(check under microscope)

b) rinse in DI water for 5 min, spin dry

**12 Prefurnace Clean**

Standard RCA clean

**13 Screen Oxide growth**

Wet Oxide, 1050 degree C

2000 angstrom

**14 Mask #3, P-well**

a) bake 110 degree C, 15 min.

b) HMDS, 4.0K, 30 sec.

c) AZ 1813, 4.0K, 30 sec, 1.3um

d) softbake, 90 degree C, 30 min

e) expose, 5.0mW/cm<sup>2</sup>, 12 sec

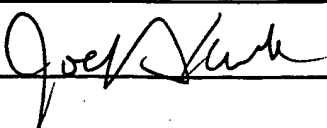
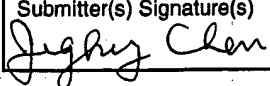
f) develop MF319, 1 min

g) rinse DI water 5 min, spin dry

h) hardbake 110 degree C, 30 min.

**15 Etch Oxide**

BHF, 9-10 min

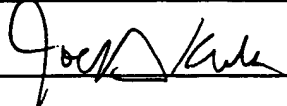
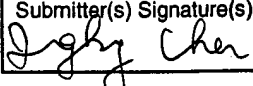
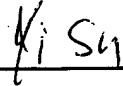
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		2/23/01
Submitter(s) Signature(s)		Date
 q/i Sn		2/23/01



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	DI water rinse, 5 minutes (hydrophobic)	1060 angstrom/min
16 p-well implant (add one n-type blank monitor wafer)	p-well ion implantation, boron, $7 \times 10^{12}/\text{sq}$ , 50keV	
17 well drive in (put in the monitoring wafers from step 6, 10, 12)	1200 degree C, 300 minutes 80%N <sub>2</sub> , 20%O <sub>2</sub> standard ramp (measure sheet resistance of the monitoring wafers)	
18 strip oxide	BHF etch, 10 minutes DI water rinse, 5 minutes spin dry	hydrophobic
(Start of LOCOS)		
19 Prefurnace clean (add two monitor wafers)	standard RCA clean	
20 Pad oxide growth	C2, DWD/TCA (DWDSKIN) 900 degree C, 5-17-10.5-5-5 TCA: LoN <sub>2</sub> =25sccm (inspect oxide thickness)	500 angstrom
21 LPCVD Nitride Deposition (put in the monitor wafers from step 17)	C4,CVD NITR (CVD) 820 degree C (check latest dep rate)	1200 angstrom
22 mask #4, active	photolithography process, AZ1813	
23 Etch nitride	RIE, check etch rate (do not strip photoresist)	
24 channel stop implant	Borob, $2 \times 10^{12}/\text{sq}$ , 150keV	
26 strip photoresist	strip photoresist, hot PRS 2000, 30 min DI water rinse, 5 minutes spin dry	
27 Prefurnace clean (add 2 monitor wafer)	standard RCA clean	
28 Field Oxidation	C2, DWD/TCA (DWDSKIN)	

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Submitter(s) Signature(s)	 	Date 2/23/01





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5-5-4:00-5-0.30, 1000 degree C  
TCA:LoN2=30sccm  
standard ramp

1.15um

(inspect oxide thickness of monitor wafers)

**29 Remove oxide on nitride**

BHF, 30 seconds  
DI water rinse, 5 minutes  
spin dry

**30 strip nitride**

hot phosphoric acid at 180 degree C  
DI water rinse 5 minutes, spin dry

100 angstrom/min

**31 Etch pad oxide  
(END of LOCOS)**

BHF, 30 seconds  
DI water rinse, 5 minutes, spin dry

**32 Prefurnace clean  
(add one monitor wafer)**

Standard RCA clean

**33 Sacrificial oxide growth**

1000 degree C

950 angstrom

**34 Threshold adjust implantation**

Boron, 2e12/sq, 50 keV, blanket implant

**35 Strip oxide**

BHF dip, 70 seconds  
DI water rinse, 5 minutes, spin dry

hydrophobic

**36 Prefurnace clean  
(add three monitor wafers)**

standard RCA clean

**37 Grow gate oxide**

C2, DA1 (oxidize)  
950 degree C, 35 minutes in dry O2/2%HCL  
(check uniformity and thickness)

350 angstrom

(GO STRAIGHT to LPCVD poly tube)

**38 Deposit CVD poly  
(GO STRAIGHT to B3)**

C3, low poly (CVD)

6000 angstrom

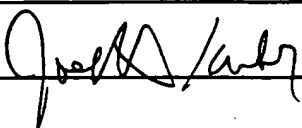
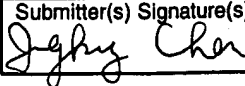
**39 Dope poly**

a) Arsenic implant 5e15/sq, 70 keV  
b) Anneal poly, 900 degree C, 30 minutes, O2

**40 Deglaze**

BHF, 60 seconds  
DI water rinse 5 minutes, spin dry

(check poly sheet resistance)

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		2/23/01
Submitter(s) Signature(s)		Date
 Yi Su		2/23/01



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41 Mask # 5 Poly	AZ1813
42 Etch poly	RIE, rotate wafers during etch
43 Strip photoresist	Hot PRS 2000, 30 minutes DI water rinse 5 minutes, spin dry
44 mask #6 pbody	photolithography, AZ 1813
45 pbody implant (add three monitor wafers)	Boron, 3 splits b1) 2.0E13/sq, 100keV
46 strip photoresist	Hot PRS2000, 30 minutes DI water rinse 5 minutes, spin dry
44 Prefurnace clean	standard RCA clean
45 pbody anneal	1150 degree C inert with 1%O2, 200 minutes
46 Mask #7 Nplus	photolithography, AZ1813
47 Phosphorus source/drain implant	Phosphorus, 4.0e15/sq, 70keV
48 Strip photoresist	hot PRS2000, 30 minutes DI water rinse 5 minutes, spin dry.
49 Mask #10 Pplus	photolithography, AZ 1813
50 p+ source/drain implant	Boron, 1e15/sq, 50keV
51 Strip photoresist	Hot PRS 2000, rinse in DI water for 5 minutes
52 Prefurnace clean (add one monitor wafers)	standard RCA clean
53 Deposit PECVD oxide	5000 angstrom
54 Anneal	900 degree C, 30 minutes, inert gas with 1% O2 standard ramp
55 Mask #8 Via1	photolithography, Az 1813
56 Open contact holes	RIE + BHF

Witnessed and Understood By

Date

Submitter(s) Signature(s)

Date

Jing Chen Yi Su

2/23/01  
2/23/01



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57 Strip photoesist

Hot PRS 2000, rinse in DI water for 5 min

58 BHF dip

30 seconds, 3 minutes DI water wash, spin dry

59 Sputter Al

Al+1/2% silicon

9000 angstrom

60 mask #8 metal

photolithography process

61 Dry Etch Al

62 Strip photoresist

Hot PRS 2000. Rinse in DI water

63 Pre-alloy clean

5 minutes acetone, hot  
5 minutes IPA, hot  
3 minutes DI water rinse  
N2 gun dry

64 Sinter

A1, Anneal-2 (Anneal-1)  
N2/H2: 90%/10%  
450 degree C, 25 minutes

Witnessed and Understood By

*Joe A. Under*

Date

2/23/01

Submitter(s) Signature(s)

*Jghy Chen* *Yi Su*

Date

2/23/01



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**People** List names of others known to have worked on this or a similar invention

None

**Related concepts** Check the Xerox Patent data base at <http://comip.wrc.xerox.com/comip/icbuhome.nsf>  
What have you found in a data base search of the topic? Give patent or IP number of the most relevant items.

None

**Prototype** Has a model, a prototype, or experiment of the invention been built, made, run or tested? ☒ Yes ☐ No

Fabrication run in progress in 201/ISBU

**Xerox product** Is the invention used by Xerox or is there a definite plan for use in a future product(s)? ☐ Yes ☐ No  
If so, please identify the program(s) or product(s), and introduction dates:

Not currently planned for a product program.  
Could be used in the future for MEMS test

**Disclosures** Has this concept been disclosed to vendors, consultants, outside parties, partners, etc? Indicate the date(s) of any previous or planned future disclosure external to Xerox, and identify the type of disclosure (by agreement, demonstration, paper or presentation given, market probe, published article, etc., and if convenient, please provide a copy of the agreement, paper or article):

Concept will be disclosed to Standard MEMS, Inc. as a part of our ATP proposal

**Outside funding** ☒ YES (Indicate Source of outside funding) ☐ NO

Research performed as a part of NIST Cooperative Agreement Number: 70NANB8H4014

Witnessed and Understood By

*[Signature]*

Date

2/23/01

Submitter(s) Signature(s)

*[Signature]* Yi Su

Date

2/23/01



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# Patent Management Technical Categories

IPA10283

(Touch the hi-lighted areas to receive a definition of the category.)

<b>Architecture and Document Services</b> <ul style="list-style-type: none"><li>1.1 Advanced Print Services</li><li>1.2 Document Access &amp; Management</li><li>1.3 Document Capture &amp; Analysis</li><li>1.4 Document Systems Architecture</li><li>1.5 Electronic Document Commerce</li><li>1.6 Networked Document Systems</li><li>1.7 Productivity Initiatives</li><li>1.8 Process, Workflow, Information Management</li><li>1.9 Smart Design &amp; Service</li><li>1.10 Work Process Analysis</li></ul>	<b>Digital Imaging</b> <ul style="list-style-type: none"><li>2.1 Capture</li><li>2.2 Presentation</li><li>2.3 Manipulation</li><li>2.4 Representation</li><li>2.5 Systems</li></ul>
<b>Marking &amp; Devices</b> <ul style="list-style-type: none"><li>3.1 Latent Image Formation (Re-Imageable Process)</li><li>3.2 Development (Re-Imageable Process)</li><li>3.3 Image Transfer &amp; Fixing (Re-Imageable Process)</li><li>3.4 Erase And Cleaning (Re-Imageable Process)</li><li>3.5 Fixed Image Marking (Incl. Direct To Plate)</li><li>3.6 Imager (ROS, Optics, Modulator, Illumination)</li><li>3.7 Thermal Ink Jet</li><li>3.8 Acoustic Ink Jet</li><li>3.9 Continuous Ink Jet</li><li>3.10 On Demand Powder</li><li>3.11 Other Direct Marking</li><li>3.12 Controls &amp; Diagnostics (For Marking Systems)</li><li>3.13 Media Handling (Feeding, Transport, Finishing)</li><li>3.14 Marking System Integration &amp; Architecture</li><li>3.15 Marking Hybrid Processes</li><li>3.16 Display Devices</li><li>3.17 MEMS Devices</li><li>3.18 Data Recording Devices</li><li>3.19 Digital Image Scanning</li></ul>	<b>Materials &amp; Materials Manufacturing</b> <ul style="list-style-type: none"><li>4.1 Toner, Developer and Components (For Re-Imageable Process)</li><li>4.2 Photoreceptors and Components</li><li>4.3 Dielectric Receivers</li><li>4.4 Inks For Direct Marking</li><li>4.5 Powders For Direct Marking</li><li>4.6 Substrate Media (Paper, Transparencies, etc.)</li><li>4.7 Electronic Materials (Light Emitting Or Detecting, Semiconductors For Printhead Or Other Use)</li><li>4.8 Display Materials</li><li>4.9 Materials for Fusing</li><li>4.10 Drum And Belt Substrates</li><li>4.11 Materials for Binding and Finishing</li><li>4.12 Materials of Controlled Conductivity</li><li>4.13 Transfix Belt</li><li>4.14 Intermediate Transfer Belts</li><li>4.15 Magnetic Materials</li><li>4.16 Recording Media</li><li>4.17 Packaging Materials</li></ul>
<b>Manufacturing Technology &amp; Product Elements</b> <ul style="list-style-type: none"><li>5.1 Component Development</li><li>5.2 Manufacturing Processes</li><li>5.3 Production Systems</li><li>5.4 Industrial Design / Human Factors</li><li>5.5 Device Electronics</li><li>5.6 Product Packaging</li></ul>	<b>Speculative Research</b> <ul style="list-style-type: none"><li>6.1 Document Futures</li><li>6.2 Applications outside Defined Xerox Direction</li></ul>



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## Manager's Comment Section

IPA10283

Submitter(s): Jingkuang Chen & Yi Su	
Title of Invention: An IC process for integration of CMOS with Lateral DMOS & Photo diode	
Manager's Name: Joel Kubby	Date: 2/23/01
1. Problem addressed or function provided by the invention: <i>Example 1A: Finisher cost reduction</i> Microelectronic integrated with MEMS devices <i>Example 1B: Uses low cost LCD to write annotation messages</i>	
2. Central thrust of the invention: <i>Example 2A: Design incorporates fewer parts</i> Design leads to higher levels of integration for optical MEMS devices <i>Example 2B: Uses low cost LCD to write annotation messages</i>	
3. Could invention have impact beyond current description? <i>Example 3A: Could also function for printer finisher</i> Could also be used for MEMS control electronics <i>Example 3B: Could also function to erase/edit copy</i>	
4. Potential for Xerox application. Specify product or technology program if possible: <i>Example 4A: Mainline approach in Program Q</i> not currently out looked for a Xerox product program. <i>Example 4B: Adds significant feature to future products</i>	
5. Value to competitors; potential for license or trade: <i>Example 5A: Enables much lower cost finishing than any known system and opens possibilities of moving finishing down-market</i> Lower cost by higher levels of integration <i>Example 5B: Could be licensed in a business area un-related to Xerox</i>	
6. Please indicate any related patents, publications, or activities you know of: None	
7. I would recommend the following form(s) of protection: <input checked="" type="checkbox"/> Patent <input type="checkbox"/> Defense publication <input type="checkbox"/> Keep trade secret <input type="checkbox"/> None	
Comments:	